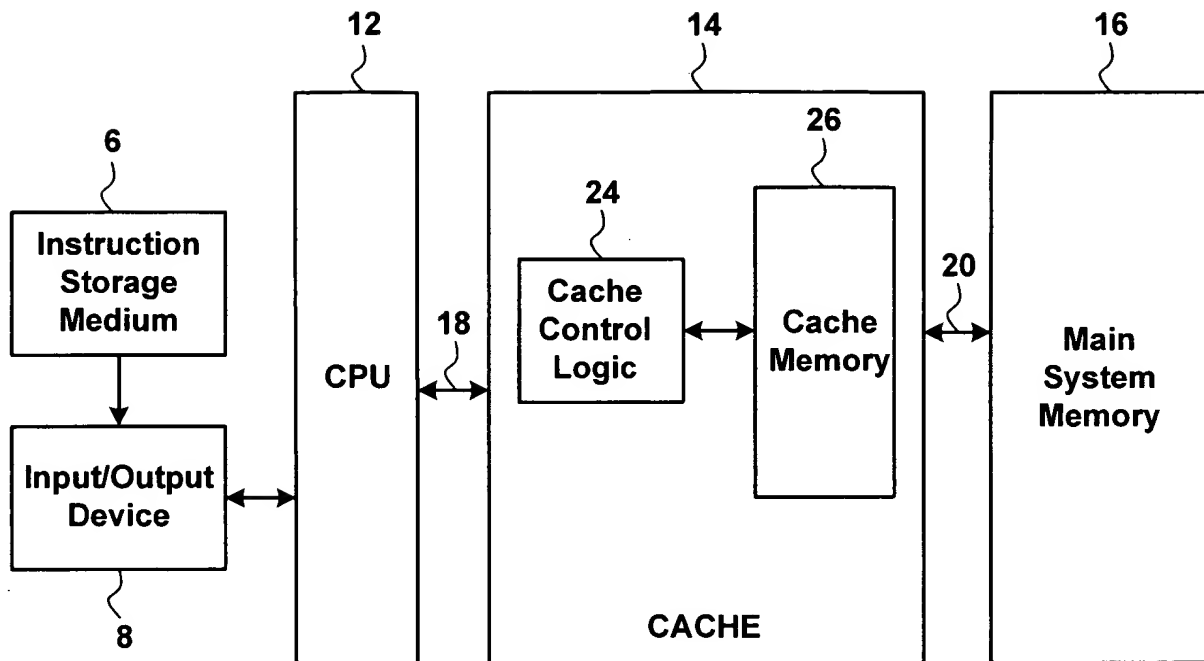


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**Figure 1**

P	30	31	32	33	34	35	36	37	38	39	40	41
Sequence	a	b	a	c	d	b	b	b	e	a	c	d
Allocation	a=>0	b=>1		c=>2	d=>3				e=>0	a=>2	c=>3	d=>1
LRU=>	1/x	2/y	2/y	3/z	1/b	0/a	0/a	0/a	2/c	3/d	1/b	0/e
R	2/y	3/z	3/z	1/b	0/a	2/c	2/c	2/c	3/d	1/b	0/e	2/a
S	3/z	0/a	1/b	0/a	2/c	3/d	3/d	3/d	1/b	0/e	2/a	3/c
T	0/a	1/b	0/a	2/c	3/d	1/b	1/b	1/b	0/e	2/a	3/c	1/d
U	w==>	x==>		y==>	z==>				a==>	c==>	d==>	b==>
V	Replaced											

**Figure 2**  
**(Prior Art)**

P	Sequence	a	b	a	c	d	b	RICL (b)	e	a	c	d
Q	Allocation	a==>0	b==>1		c==>2	d==>3			e==>1			
LRU=>	0/w	1/x	2/y	2/y	3/z	1/b	0/a	1/b	0/a	2/c	3/d	1/e
R	1/x	2/y	3/z	3/z	1/b	0/a	2/c	0/a	2/c	3/d	1/e	0/a
S	2/y	3/z	0/a	1/b	0/a	2/c	3/d	2c	3/d	1/e	0/a	2/c
T	3/z	0/a	1/b	0/a	2/c	3/d	1/b	3/d	1/e	0a	2/c	3/d
U	Replaced	w==>	x==>		y==>	z==>			b==>			
V												

37

38

Importance level of cache line is reduced; cache line b continues to store valid data

Figure 3